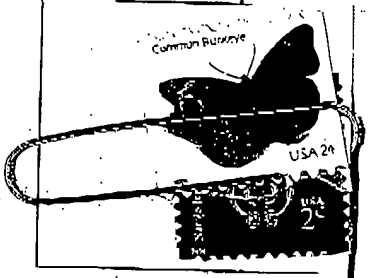
Docket No. 501299.01

EWB:gah

Date Stamp



Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SENT: April 3, 2008

Kindly acknowledge receipt of the below-listed documents by placing your receiving stamp hereon and mailing:

**Request for corrected Certificate of Correction; Original Certificate of Correction (with changes marked in red) in re: Tae H. Kim, U.S. Patent No. 6,975,552 B2, Issued December 13, 2005, for HYBRID OPEN AND FOLDED DIGIT LINE ARCHITECTURE.**

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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 3, 2008 Jennifer A. Steele

Date Jennifer A. Steele

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Applicant | : Tae H. Kim | Attorney Docket No. | : 501299.01 |
| Patent No. | : US 6,975,552 B2 | Serial No. | : 10/644,610 |
| Issue Date | : December 13, 2005 | Filed | : August 19, 2003 |
| Title | : HYBRID OPEN AND FOLDED DIGIT LINE ARCHITECTURE | | |

## REQUEST FOR CORRECTED CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is the original official Certificate of Correction received from the PTO in the above-identified application, for which issuance of a corrected Certificate of Correction is respectfully requested.

There is an error with respect to the following data, which is incorrectly omitted.

| Column, Line | Reads | Should Read |
|---|---|---|
| Item (57), Line 3 | "and open line" | --and open digit line-- |
| Column 7, Line 38 | "of the memory arrays **202***a*, **202***b* is a respective row address latch **226**, which stores the row address, and a row decoder **228** which applies various" | --of the memory arrays **202***a*, **202***b* is a respective row address latch **226**, which stores the row address, and a row decoder **228**, which applies various-- |

The corrections to be made have been marked in red on the original of the enclosed Certificate of Correction.

Respectfully submitted,

DORSEY & WHITNEY LLP

Edward W. Bulchis
Registration No. 26,847

EWB:gah
Enclosures:
Postcard
Original Certificate of Correction (with changes marked in red)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Tel: (206) 903-8800
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h:\ip\clients\micron technology\1200\501299.01\501299.01 req corrected cert of corr.doc

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO. : 6,975,552 B2
APPLICATION NO. : 10/644610
DATED : December 13, 2005
INVENTOR(S) : Tae H. Kim

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

| Column, Line | Reads | Should Read |
|---|---|---|
| Item (57), Line 3 | "and an open digit line" | --and open digit line-- |
| Column 1, Lines 45, 50 and 52 | "complimentary" | --complementary-- |
| Column 2, Line 40 | "pair is surrounded" | --pair being surrounded-- |
| Column 4, Line 30 | "to which portion of a digit line memory cells are" | --to which portions of a digit line of memory cells are-- |
| Column 4, Line 41 | "aspects of a open digit line" | --aspects of an open digit line-- |
| Column 4, Line 64 | "array **10**, thus, coupling" | –array **10**, thus coupling-- |
| Column 5, Line 57 | "memory arrays, thus," | --memory arrays, thus-- |
| Column 5, Line 59 | "to active column **50, 80**" | --to active columns **50, 80**-- |
| Column 6, Line 27 | "but are instead, shifted" | –but are instead shifted-- |
| Column 6, Line 41 | "are desired. For example," | --are desired; for example,– |

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO. : 6,975,552 B2
APPLICATION NO. : 10/644610
DATED : December 13, 2005
INVENTOR(S) : Tae H. Kim

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

| | | |
|---|---|---|
| Column 6, Line 66 | "MDL portion **156.** virtue of the data state stored by the" | –MDL portion **156.** Consequently, the voltage of the digit line will be altered from the precharge voltage by virtue of the data state stored by the-- |
| Column 7, Line 38 | "of the memory arrays **202***a*, **202***b* is a respective row various" | --of the memory arrays **202***a*, **202***b* is a respective row address latch **226**, which stores the row address, and a row decoder **228**, which applies various– |
| Column 14, Line 21 | "cells of the column" | --cells of the column-- |

Signed and Sealed this

Twenty-fifth Day of December, 2007

JON W. DUDAS
*Director of the United States Patent and Trademark Office*